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EXAMINER	
WILLIAMS, HOWARD L	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/661,287
Filing Date: September 12, 2003
Appellant(s): CHEN, FENG

Jay Cantor
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 23 February 2006 appealing from the Office action mailed 06 January 2006

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Non-Patent Literature

Benabes, P. et al., "Passive Sigma-Delta Converters Design", IEEE Instrumentation and Measurement Tecnology Conference Record, Anchorage, AK., 21-23 May 2002, pages469-474

Chen, F., et al. "A 0.25-mW Low-Pass Passive Sigma-Delta Modulator with Built-In Mixer for a 10-MHz IF Input", IEEE Journal of Solid-State Circuits, Vol. 32, No. 6, June 1997, pages 774-782.

U.S Patents

5,227,795	Yamakido et al.	07-1993
5,103,228	Voorman et al.	04-1992

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 1-4, 6-12, and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Benabes et al. article (*Passive sigma-delta converter design*) in view of the Chen et al. IEEE Journal of Solid State Circuits article (*A 0.25 mW 13 b passive ΣΔ modulator with a Built-In Mixer for a 10 MHz IF input*) and Yamakido et al.

(US 5,227,795) or Voorman et al. (US 5,103,228). Benabes et al. article *Passive Sigma-Delta Converters Design* discloses a delta-sigma ADC with a continuous time passive filter (fig. 3 page 471). Benabes et al. also discloses a discrete time feedback circuit via the DAC shown in figure 1 (page 469). Benabes et al. shows in figure 2 a model of the feedback loop, input is taken as zero for figure 2, shown as a switch and hold element which is seen as reasonably suggestive of a capacitor for the hold element. Chen et al. discloses use of passive filtering delta-sigma ADC using switched capacitors in the feedback loop. Use of switched capacitor as the DAC feedback element in Benabes would have been obvious to provide a simple and compact DAC and the use of RC passive filters would provide reduced switching noise. Benabes et al. and Chen et al. don't specify whether the respective input signals are a voltage or a current signal so they don't disclose a transconductance element. Yamakido et al. and Voorman et al. disclose transconductance elements (V-I) to provide a current for summing with the fedback signal. The inclusion of a transconductance element in Benabes et al. would have been obvious because current summing is faster and more simply implemented than voltage summing.

(10) Response to Argument

At the outset the examiner notes that it is irrelevant that the Chen article is authored by the present applicant because it clearly predates the present application by more than one year and deals with very similar subject matter.

Appellants argument that Benabes does not disclose passive filters lacks merit. First, the argument is contradicted on page 5 of the Appellants brief in reference to Benabes et al. figure 3 where it reads "However, this figure is merely a showing of a filter using all passive elements."

Yes, Benabes et al. shows a second order passive filter in figure 3 --or two first order filters connected to each other to form a second order filter-- to provide a desired transfer function G(s) (see equation 7). This filter is intended to be the filter G(s) in figure 1 where it is represented in block form. The fact that Benabes et al. provides a depiction of the overall circuit in separate figures with some in block format and other providing more detailed drawings of particular components does not strike the examiner as a solid basis for Appellants' argument.

As for the remarks on page 4 regarding Benabes et al. and column 1 of their article this point is not found persuasive either. The second paragraph in the Introduction second does make reference to the Leung/Chen article but it seems an enormous leap to argue that Benabes does not disclose a passive circuit on their own. In the last paragraph in column 1 and spanning to column 2 Benabes et al. note they will examine continuous time filters and continuous-time filters in ΣΔ (sigma-delta) modulators "using only resistors and capacitors elements" or in other words passive filters. Benabes et al. feedback (DAC figs. 1 & 2) is also discrete noting the clock signal as one would expect. Benabes et al. figure 2 is shown with the supposition of an input signal equal to zero so that the feedback signal is, for that example, the only signal received. This figure represents the DAC as a sample and hold supplying the filter G(s). The hold element is readily implemented as a capacitor and the first switch clearly makes it discrete. Thus the Benabes et al. article is seen to disclose a discrete time feedback circuit.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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